BIT-3000
Dynamic Sequencing Generator and Analyzer

Datasheet 1.20

BitifEye
Digital Test Solutions

BitifEye Digital Test Solutions GmbH
Herrenberger Strasse 130
71034 Boeblingen, Germany

info@bitifeye.com
www.bitifeye.com

Notices

Edition

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Product Labels


This electronic product is in compliance with the EMC and Safety regulations of the European Community.


Read the instructions in the BIT-3000 manual, as well as this datasheet, before using this electronic product.


This electronic product must be operated with AC power.

Technical Assistance

If you need product assistance or if you have suggestions, contact BitifEye. You will find the contact information on the BitifEye homepage at:

http://www.bitifeye.com

Representatives of BitifEye are available during standard German business hours.

Before you contact BitifEye, please note the actions you took before you experienced the problem. Then describe those actions and the problem to the technical support engineer.

Find a Mistake?

We encourage comments about this publication. Please report any mistakes to BitifEye (support@bitifeye.com)

Contents

Focus

This datasheet applies to the BIT-3000 Dynamic Sequencing Generator and Analyzer. The following components are covered by this document:

Description	Product Number	Article Number
BIT-3000 Series DSGA Platform Mainframe	BIT-3000A	BIT-4000-3000-0
BIT-3000 Series DSGA Platform Mainframe	BIT-3000B	BIT-4000-3000-1
BIT-3000 Series DSGA Platform Clock Module	BIT-3001A	BIT-4000-3001-0
BIT-3000 Series DSGA Platform Clock Module	BIT-3001B	BIT-4000-3001-1
BIT-3000 Series DSGA Platform Generator Module	BIT-3002A	BIT-4000-3002-0
BIT-3000 Series DSGA Platform Generator Module	BIT-3002B	BIT-4000-3002-1
BIT-3000 Series DSGA Platform Analyzer Module	BIT-3003A	BIT-4000-3003-0
BIT-3000 Series DSGA Platform Analyzer Module	BIT-3003B	BIT-4000-3003-1
BIT-3000 Series DSGA Platform Trigger Module	BIT-3004A	BIT-4000-3004-0
BIT-3000 Series DSGA Platform Trigger Module	BIT-3004B	BIT-4000-3004-1
BIT-3000 Series DSGA Platform Relay Module	BIT-30R22B	BIT-4000-3022-1
BIT-3000 Series DSGA Platform Solid State Switch Module	BIT-30S22B	BIT-4000-3023-1

This datasheet is only intended to provide the user a quick overview of the features and regulations of the instrument. For detailed information about usage, please refer to the BIT-3000 User Manual (available from the BitifEye website, http://bitifeye.com).

1. Electrical Specifications

Supply

Supply Voltage	110–240 V AC, 50–60 Hz
Electrical Power	80 W
Overvoltage Category	II
Isolation	3 kV
Fuses	2× 1.6 A 250 V slow blow
AC Cable	Cold device cable, 3-wire with grounding terminal 0.75 mm² or 18 AWG minimum

External Clock Input

Frequency Range	10 MHz recommended typical range 5 MHz to 20 MHz
Amplitude	min. 100 mVpp, square-wave recommended max. ±2 V
Impedance	50 Ω into GND

External Clock Output

Frequency	10 MHz when using internal reference
Amplitude	typ. 950 mVp-p into 50 Ω
Load	50 Ω or more into GND

Clock

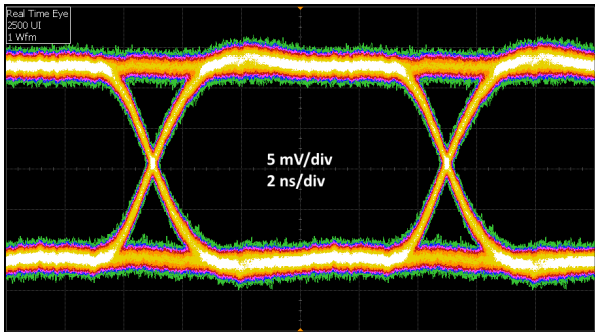
Frequency Range (PLL)	50 MHz to 100 MHz
Frequency Range (Direct Clock)	Same as external clock input
Synthesized Generator Clock Range	1 kHz to 100 MHz (digitally divided from PLL or direct clock)

Generator

Voltage Window	-3.5 V to +3.5 V
Swing	0 to 1.7 Vp-p single-ended when driving 50 Ω load 0 to 3.4 Vp-p single-ended when high-impedance load
Offset	-1.0 V to +1.0 V (relative to termination voltage) when driving 50 Ω load -3.5 V to +3.5 V when driving high-impedance load

Load	50 Ω or more into GND
Data rate	Same as clock frequency range

Typical Performance

Eye Diagram (25 mV amplitude, 100 Mbit/s)	

Analyzer

Termination	differential source: 50 Ω into GND, or 100 Ω differential single-ended source: 50 Ω into GND, or high-impedance
Input Voltage	-4 V to +4 V
Sensitivity	100 mV
Threshold	-3.5 V to +3.5 V
Data rate	up to 100 MBit/s (NRZ)

Trigger Input

Termination	50 Ω into GND, or high-impedance
Input Voltage	-4 V to +4 V
Sensitivity	recommended minimum pulse shape: 100 mV, 25 ns
Threshold	-3.5 V to +3.5 V

Trigger Output

Levels	0 V / 1 V into 50 Ω typical 0 V / 2 V into high-impedance typical
Load	50 Ω or more into GND
Pulse Width	max. 10 ms resolution 1 Bit time (same clock as generator)

Relay Switch

Insertion Loss	max. 0.8 dB at 26.5 GHz
Standing Wave Ratio	max. 1.7 at 26.5 GHz
Switch Cycles	min. 1 million
Termination	inactive path is open (reflective)

Solid-State Switch

Absolute Maximum Voltage Levels	-0.5 V to +2.0 V
Insertion Loss	max. 1.45 dB (at 0.3 GHz) max. 1.9 dB (at 3 GHz) max. 2.4 dB (at 6 GHz) max. 2.7 dB (at 8 GHz) max. 4.2 dB (at 12 GHz)
Insertion Loss Imbalance [1]	max. 2 %
Return Loss	typ. 10..20 dB (DC to 12 GHz)
Group Delay	typ. 1.01 ns ± 0.06 ns (50 MHz to 12 GHz)
Isolation	typ.37 dB max. 34 dB
Switching Time [2]	typ. 6.5 ns max. 10 ns
Switching Time Skew [3]	typ. ±0.5 ns max. ±2 ns
Saturation Limit	typ 1.2 V min. 1.15 V
Termination	inactive path is terminated with 50 Ω into GND return loss into termination typ. 12 dB, max. 10 dB
Intra-Pair Skew [4]	typ. ±1.5 ps max. ±2.5 ps
Inter-Pair Skew [5]	typ. ±2.5 ps max. ±6 ps

[1] measured by comparing the settled voltage levels of the step response (measured using VNA/TDR method)

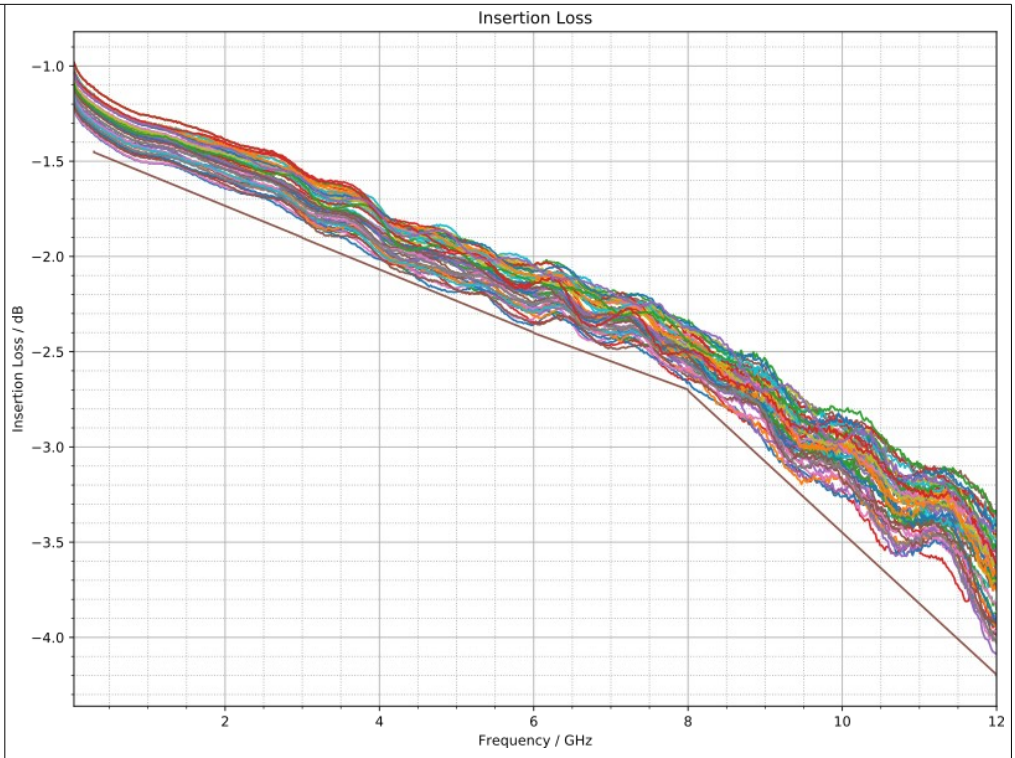
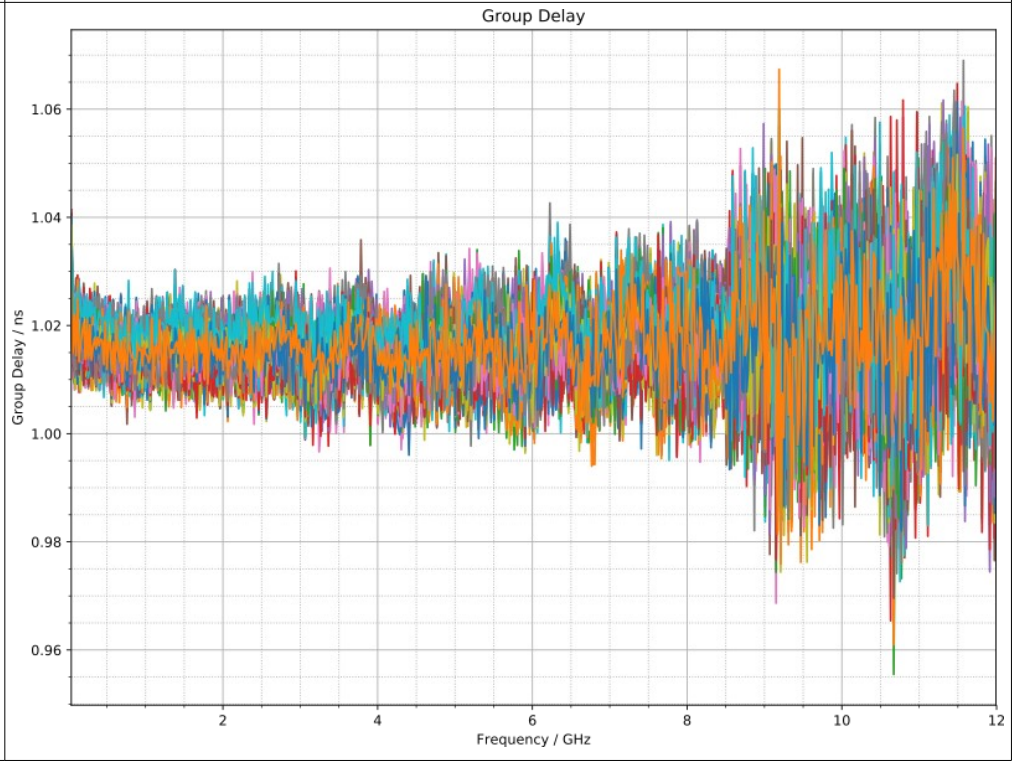
[2] during switching, both signals (1 and 2) will be attenuated for a short moment; the switching time is the time between the point when signal 1 falls below 50% and the point when signal 2 rises above 50%

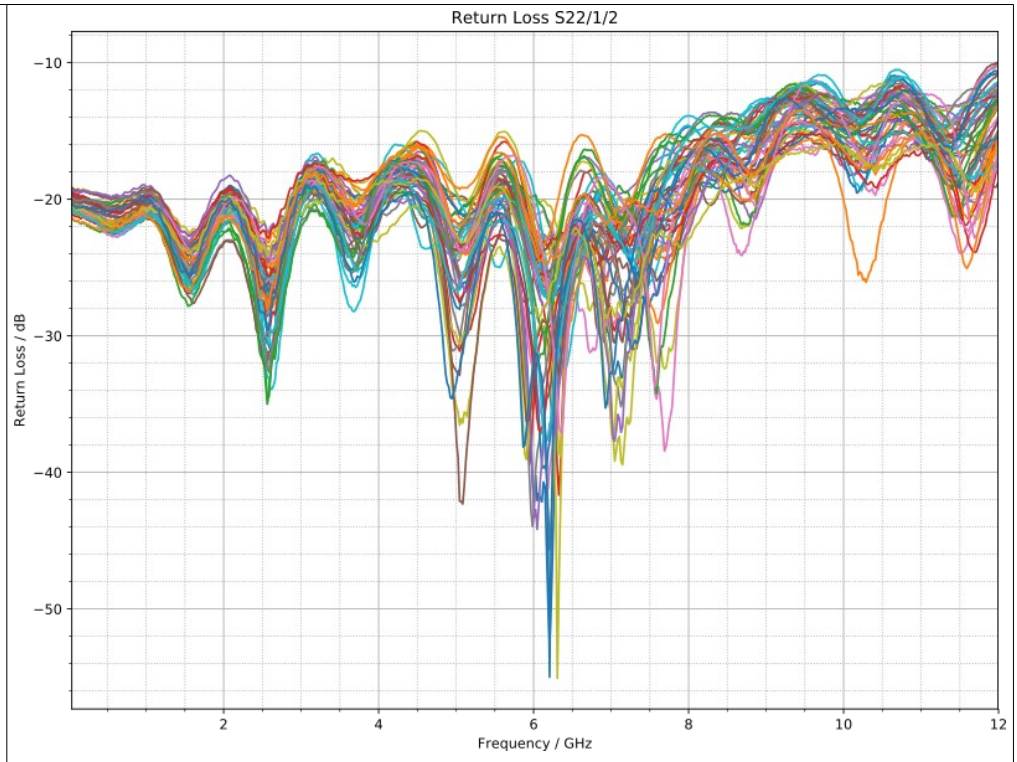
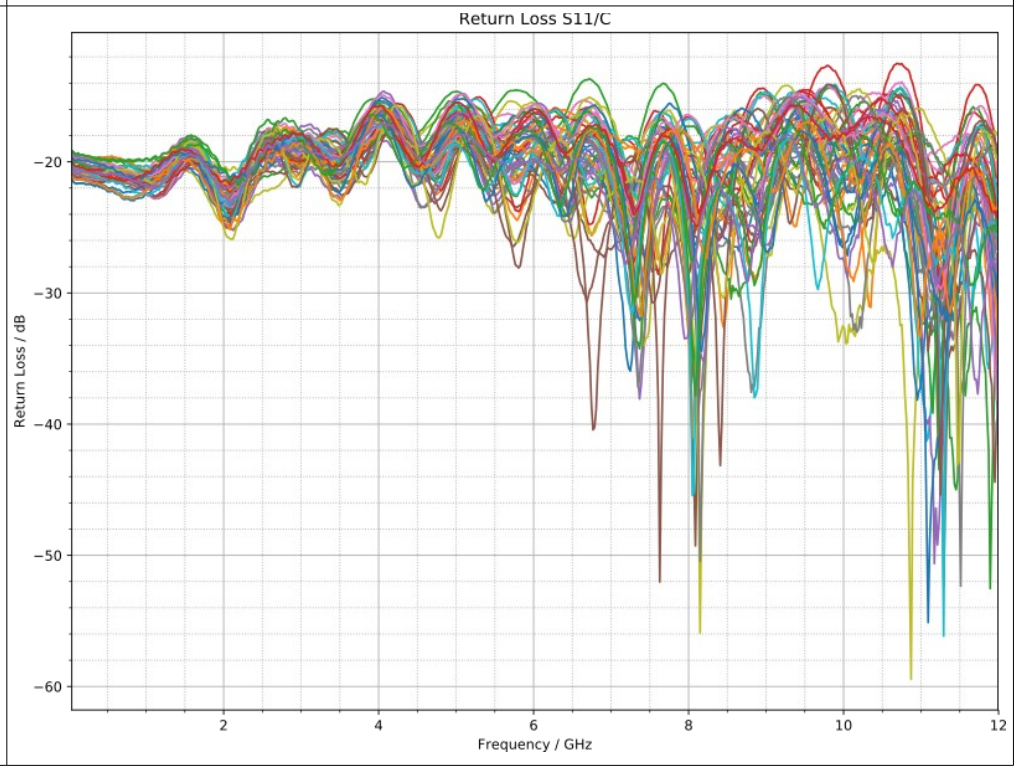
[3] the time difference between the middle of the period when switch A switches from 1 to 2, and the middle of the period when switch B switches from 1 to 2

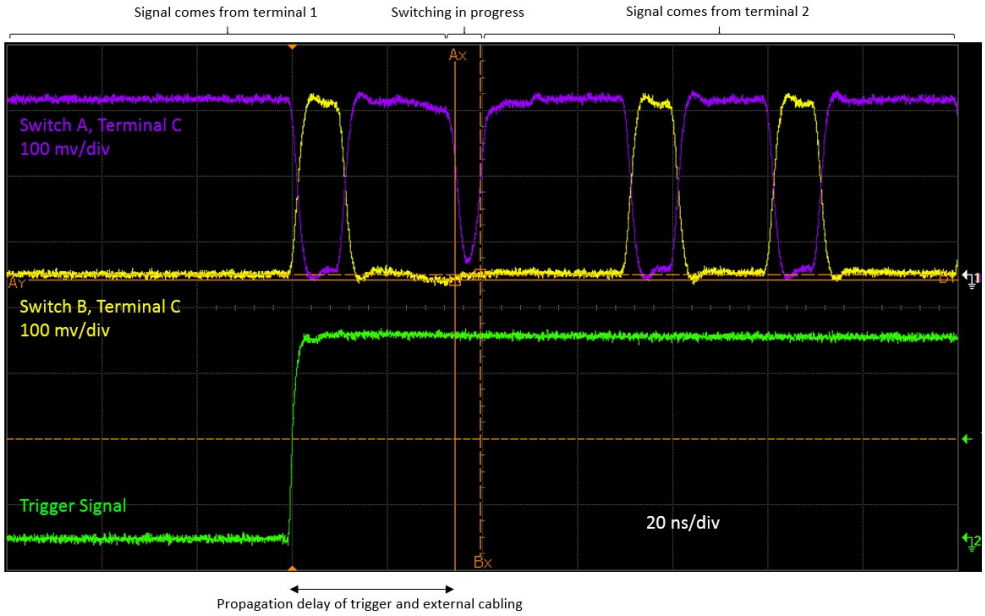
[4] the worst of the propagation time difference between path 1-C of switch A and B, and the propagation time difference between path 2-C of switch A and B (measured using VNA/TDR method)

[5] the worst of the propagation time difference between path 1-C and 2-C of switch A, and the propagation time difference between path 1-C and 2-C of switch A (measured using VNA/TDR method)

Typical Performance Plots

Insertion Loss	
Group Delay	

Return Loss (terminal 1 or 2)	
Return Loss (terminal C)	

Switching Behavior	

2. Digital Specifications

Sequencer

Loop Levels	8
Sequence Memory	512 Instructions
Pattern Memory	16 MBit per channel

Analyzer

Pattern Events	12 pattern events, 48 bit each adjacent event patterns can be combined (e.g. to create events of 96 bit up to 576 bit)
Pattern Recorder	4 recorders available 16 MBit per recorder

3. Mechanical Specifications

Physical Dimensions

Weight	Approx. 6 kg to 7 kg, depending on equipped modules
Dimensions	482 mm wide, 185 mm tall, 375 mm deep

Mounting

Ventilation	Keep min. 5 cm distance to all ventilation slots
Rack Mounting	4.5 RU minimum

4. Compliance Specifications

Environmental Conditions

Temperature	+5 °C to +40 °C (stability ±15 °C)
Humidity	up to 80% relative humidity (non-condensing)
Altitude	up to 2000 m above sea level
Pollution Degree	2

Electromagnetic Compatibility

The BIT-3000 DSGA is compliant with the following EMC specifications:

- EN 61326-1:2013
- IEC 61326-1:2012
- DIN EN 61326-1:2013

These specifications only apply when the instrument is used in accordance with this datasheet and the user manual. Only use shielded coaxial signal cables (clock, generator, analyzer, trigger, relay switch, solid-state switch) no longer than 3 m.

Safety

The BIT-3000 DSGA is compliant with the following safety specifications:

- EN 61010-1:2010
- IEC 61010-1:2010
- DIN EN 61010-1:2011

5. List Of Acronyms

AWG	American Wire Gauge
CPU	central processing unit
DSGA	dynamic sequencing generator and analyzer
EMC	electromagnetic compatibility
FPGA	field-programmable gate array
GND	ground
LAN	local area network
RU	rack unit