Keysight N5990A SATA Link Training Suite

KEYSIGHT TECHNOLOGIES

User Guide

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1 Introduction

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1.1 Overview of This Guide

This guide provides a detailed description of the N5990A SATA Link Training Suite.

1.2 Document History

First Edition (May, 2015)

The first edition of this guide describes the functionality of the software version 1.0.

1.3 SATA Link Training Suite - Overview

The SATA (Serial Advanced Technology Attachment) Link Training Suite software (short: “SATA LTS” or “software”) is a stand-alone software utility. It provides semi-automatic control of Keysight Technologies (formerly Agilent Technologies) M8020A J-BERT or N4903B J-BERT (Jitter Bit Error Ratio Tester) -based SATA generator hardware for physical layer tests. It is a flexible tool for troubleshooting and debugging. The SATA LTS complements the full Test Automation Software (Keysight N5990A opt. 103 and 203, subject to the configuration), which provides automated physical layer compliance tests and device characterization. It generates the data sequences and allows pattern changes as well as the control of signal levels, frequency, and timing parameters. The software runs on a standard Windows XP or Windows 7 PC and controls the hardware test resources through appropriate interfaces such as a LAN (Local Area Network).

2 Software Installation and Update

2.1 Software Installation / 11
2.2 Software Update / 13

If the software is already installed on the PC and is not to be updated, proceed to the next chapter Starting and Registering the Software.

2.1 Software Installation

The SATA Link Training Suite software runs on a standard PC, which is used to control the test instruments. The supported operating systems and required software to be installed prior to the SATA Link Training Suite installation are given in the following section.

2.1.1 Supported Operating Systems

The SATA Link Training Suite software is supported on the following operating systems:

- Windows XP SP2 or higher
- Windows 7

2.1.2 Software Requirements

Install the following software in the order given:

- Keysight VISA IO Library 16.3 or higher (IO_Libs_Suite folder)
- Microsoft .Net Framework redistributable 2.0 (dotnetfx20.exe)

Once the required software is ready, the SATA Link Training Suite software installer file can be executed.

The second page of the installer wizard will show the software license agreement (see Figure 2-1). Read it carefully and select “I accept the terms of the License Agreement” option. Then, click on “Next” to continue.

After pressing the “Next” button, the install location window is displayed as shown in Figure 2-2. Click the “Browse...” button to select the destination folder, in which the software shall be installed. Next, click the “Install” button to install the software.

After the installation, the SATA Link Training Suite icon will be available on your desktop (see Figure 3).

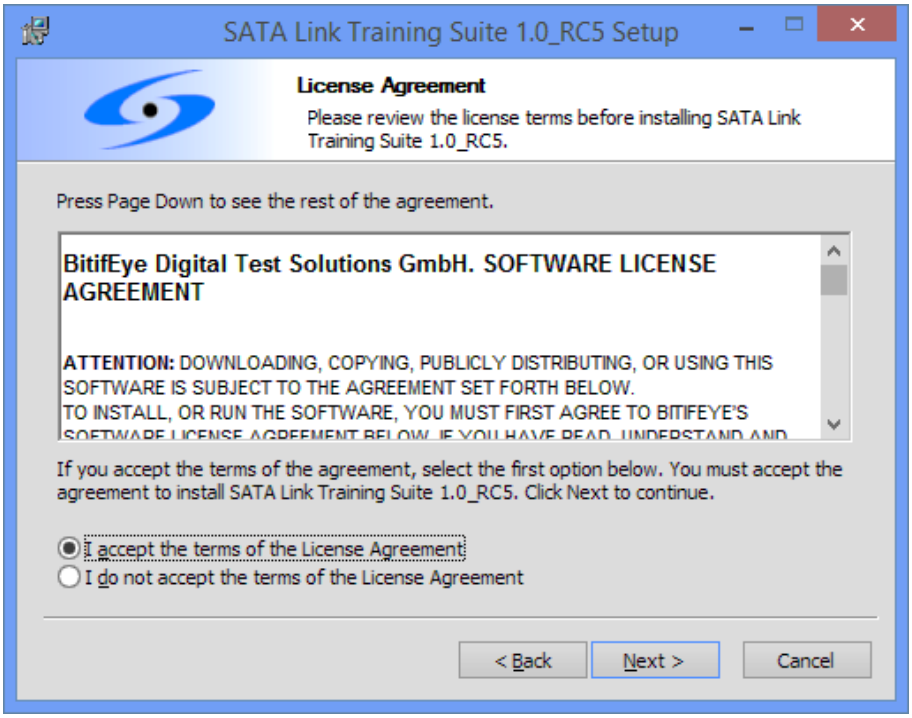

Figure 2-1: License Agreement Window

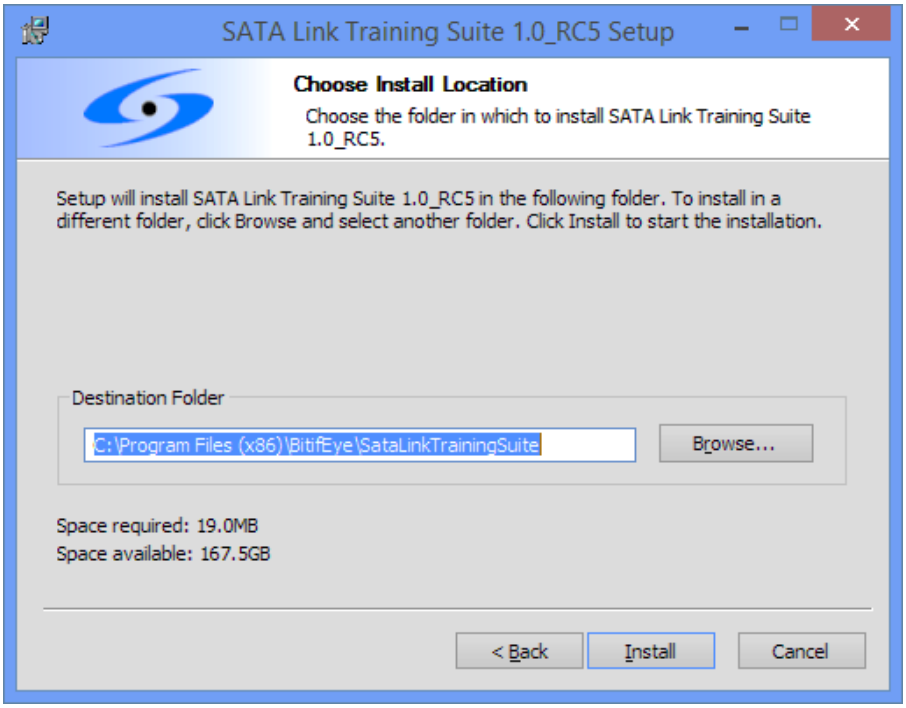

Figure 2-2: Install Location Window

After the installation, the SATA Link Training Suite icon will be available on your desktop (see Figure 2-3).

Figure 2-3: SATA Link Training Suite Icon

2.2 Software Update

If you want to upgrade a previous version of the SATA Link Training Suite software, please uninstall it first from the PC. Then continue with the chapter Software Installation.

3 Starting and Registering the Software

3.1 Starting Unregistered Software / 15
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3.1 Starting Unregistered Software

If you start the software without a valid registration key, the window shown in Figure 3-1 will open.

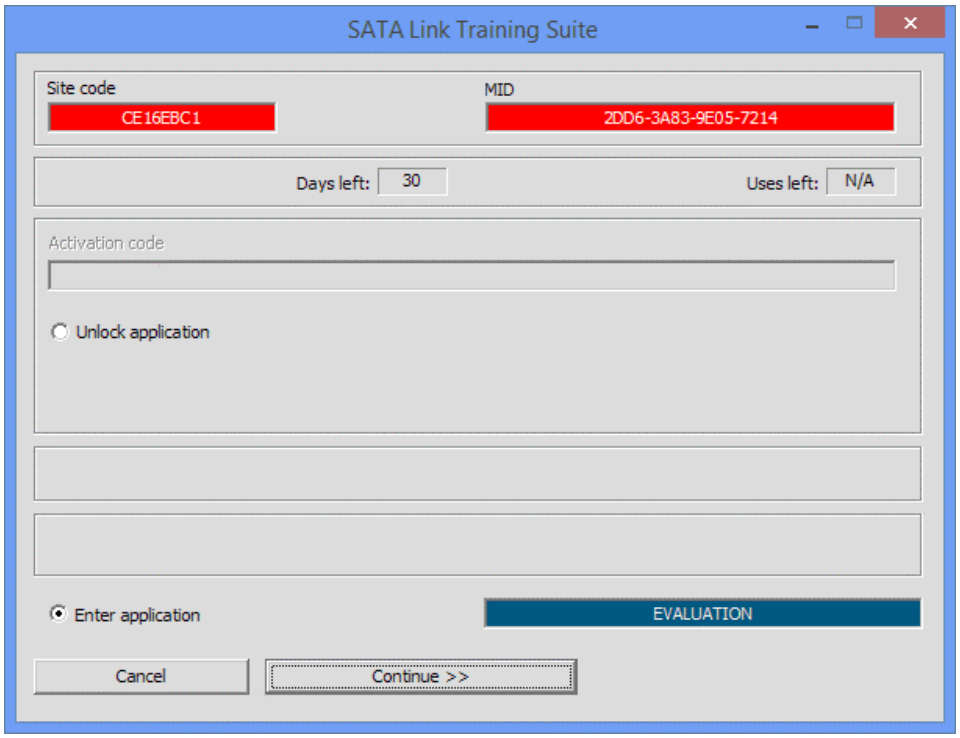

Figure 3-1: SATA Link Training Suite Registration Window

The SATA Link Training Suite can be used for 30 days without registration. Select “Continue >>” to enter the application unregistered. To register the software see below.

3.2 Software Registration

To get a registration key, send a mail to licensing@bitifeye.com with the following information:

- Customer name (such as company and department or university and institute)
- 16 digit certificate number (XXXX-XXXX-XXXX-XXXX, supplied with your N5990A / Frame Generator CD)
- Site code (read from the start window)
- Machine ID (MID, from the start window)

Your activation code will be provided within three (3) working days of your mail reaching the address indicated above.

This code is then entered into the start window shown in Figure 3-1. Select “Unlock application” and type or copy and paste your activation code into the adjacent box. Press the “Register Product” button and then “Ok”. The SATA Link Training Suite software is now ready to use.

3.3 Starting Registered Software

Double click on the SATA Link Training icon on the desktop (see Figure 2-3) or start the software from the Start / Programs / BitifEye / SATA Link Training. If you have already registered your software, it will start automatically.

4 Test Instrument Setup

4.1 N4903B J-BERT Setup / 17
4.2 M8020A J-BERT Setup / 20

Prior to using the SATA Link Training Suite software for connecting instruments, it is recommended that you set up the test instruments and establish the required connections.

- Connect the instruments to the controller PC by LAN
- Establish all required cable connections between the instruments and the UUT (unit under test).
- Switch on the PC and instruments.
- Start Keysight “IO (Input Output) VISA (Virtual Instrument Software Architecture) Connection Expert” and check the connections for the instruments.

Set the correct IP addresses of the instruments.

4.1 N4903B J-BERT Setup

The following list shows the specific instruments and accessories for the N4903B configuration:

- 1 Keysight N4903B High Performance Serial BERT
- 1 Keysight N4915-60001 ISI Channel
- 1 SATA Driver Adapter Fixture
- 2 Power Dividers (if 2 channels are selected)
- 2-6 TTCs (depending on the data rate to test)
    - For 1.5 Gbit/s: two 250 ps TTCs from Keysight (Agilent) (15432B) or 150 ps Picosecond Pulse Labs (5915-110-150ps).
    - For 3.0 Gbit/s: two 150 ps TTCs from Keysight (Agilent) (15435A) or Picosecond Pulse Labs (5915-110-150ps).
    - For 6.0 Gbit/s: two 100 ps TTCs from Picosecond Pulse Labs (5915-110-100ps).
- 8-10 SMA cables (depending on the number of channels)
- 1 NetIo 230B/C or Synaccess NP Power Distribution Unit (optional)
- 1 N4916B De-emphasis Signal Converter (optional)
- Two 11742A Blocking Capacitors (if De-emphasis Signal Converter is used)
- 1 Bias-Tee, e.g. Mini Circuits ZFBT-4R2G+ (only for hosts that need to be trained with a trigger)

The connection diagrams for 1 and 2 channels are shown in Figure 4-1and Figure 4-2 respectively.

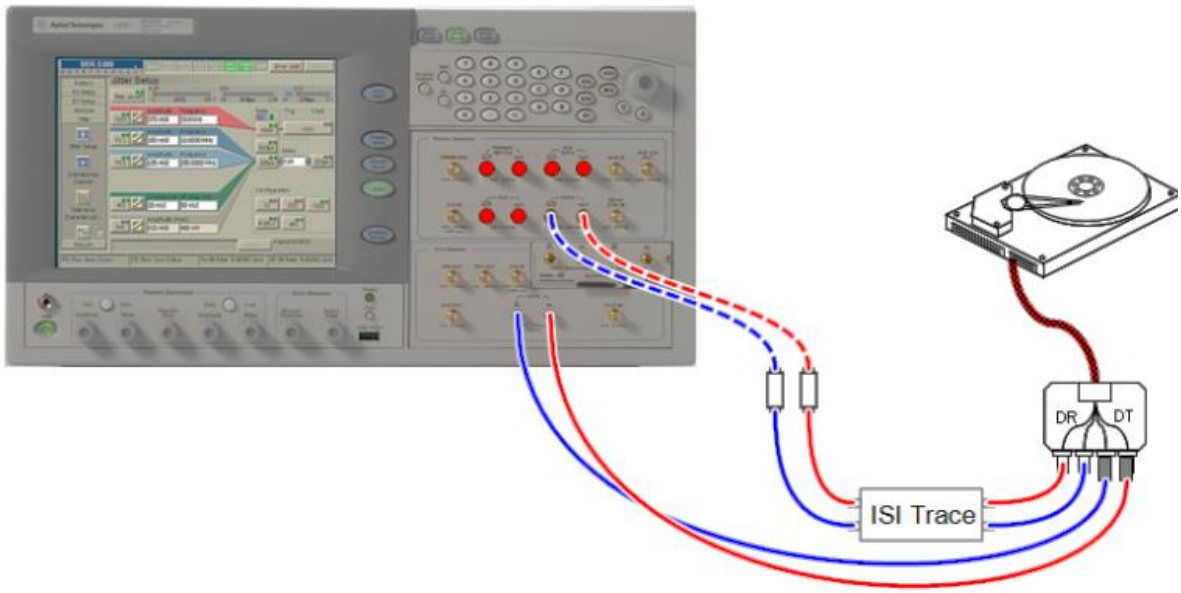

Figure 4-1: Connection Diagram for N4903B Setup with 1 Channel

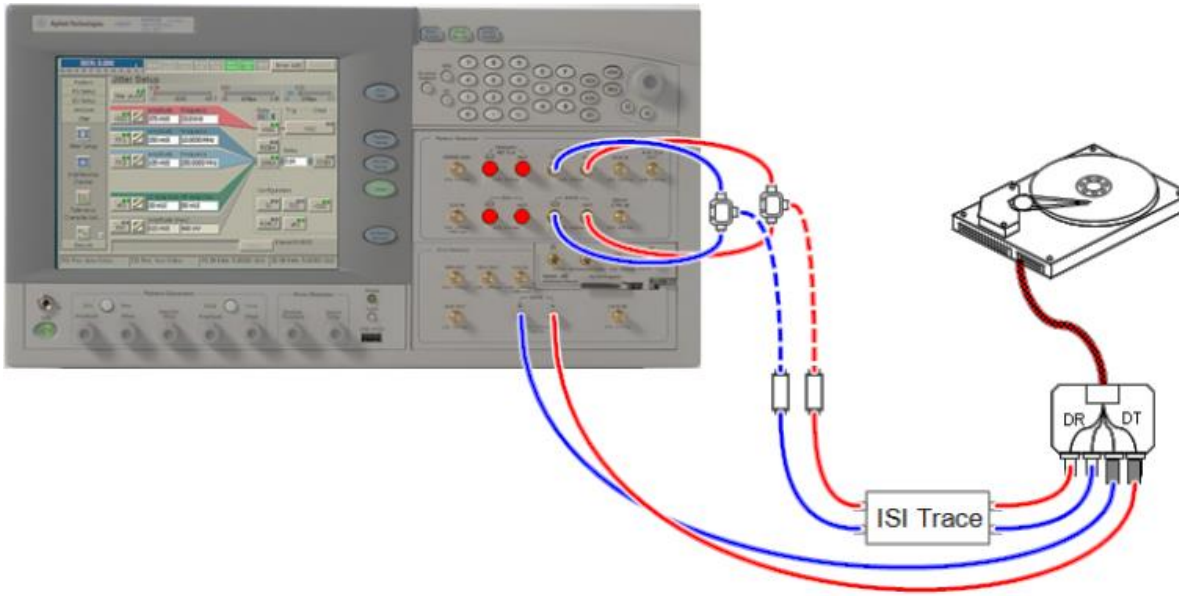

Figure 4-2: Connection Diagram for N4903B Setup with 2 Channels

4.1.1 De-Emphasis Box

An N4916B De-emphasis signal converter can be used to generate de-emphasized signals (see connection diagram in Figure 4-3). The N4916B must be connected to the J-BERT via USB. This option is only available when 1 channel is selected.

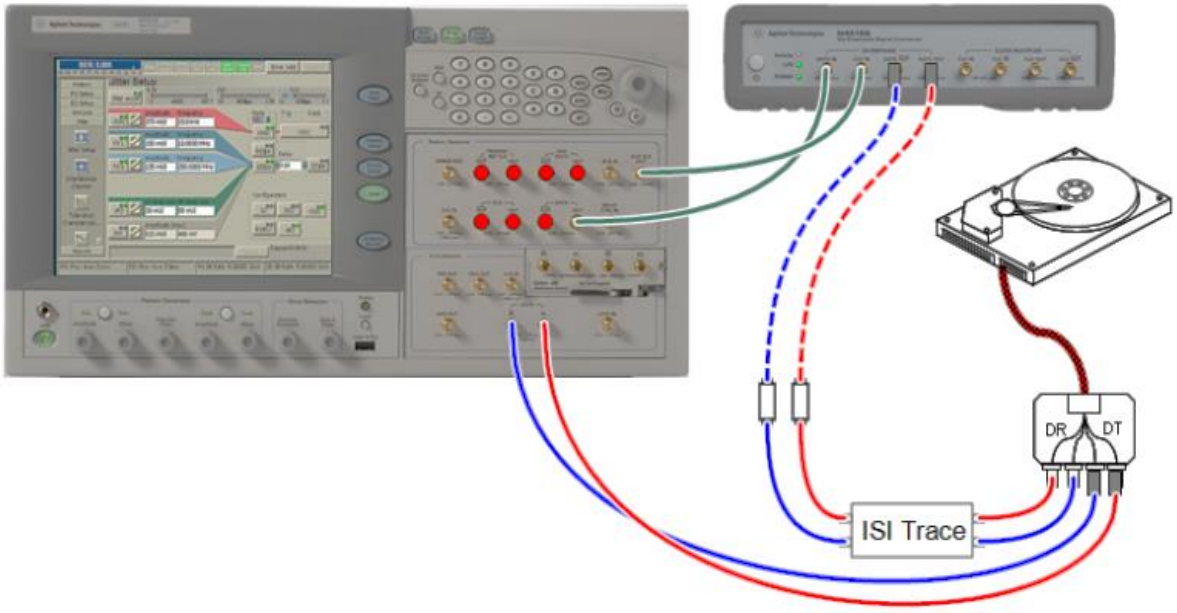

Figure 4-3: Connection Diagram for N4903B Setup with De-emphasis Box

4.1.2 With Trigger

When the UUT is a host, the training sequence can be started by using the trigger input as shown in Figure 4-4. A Bias-Tee (e.g. Mini Circuits ZFBT-4R2G+) is required.

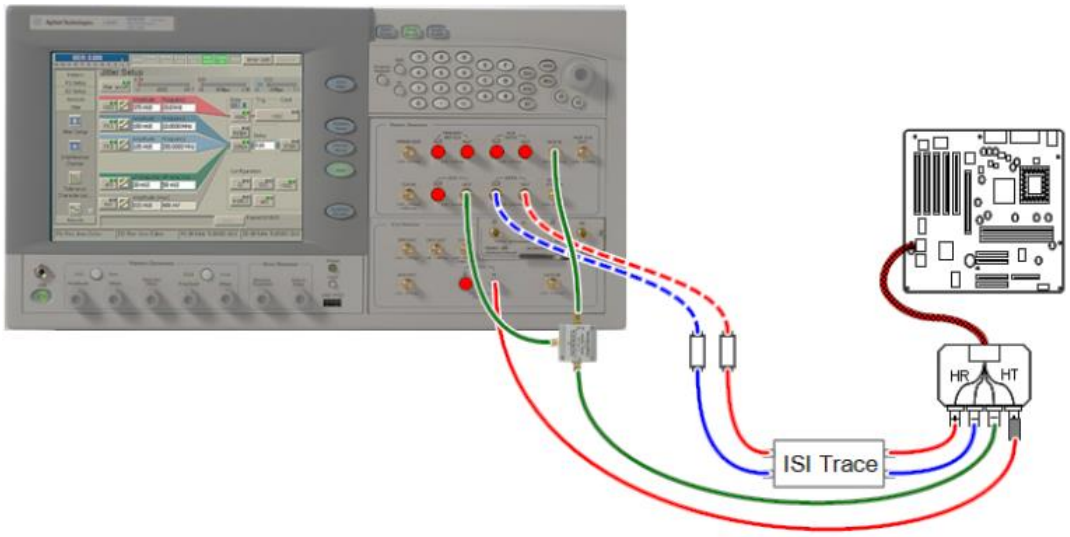

Figure 4-4: Connection Diagram for N4903B with Trigger (Host)

4.2 M8020A J-BERT Setup

The following list shows the specific instruments and accessories for the M8020A configuration:

- 1 Keysight M8020A High Performance BERT
- 1 Keysight N4915-60001 ISI Channel
- 1 SATA Driver Adapter Fixture
- 2 Power Dividers (when 2 channels are selected)
- 2-6 TTCs
    - For 1.5 Gbit/s: two 250 ps TTCs from Agilent (15432B) or 150 ps Picosecond Pulse Labs (5915-110-150ps).
    - For 3.0 Gbit/s: two 150 ps TTCs from Agilent (15435A) or Picosecond Pulse Labs (5915-110-150ps).
    - For 6.0 Gbit/s: two 100 ps TTCs from Picosecond Pulse Labs (5915-110-100ps).
- 6-10 SMA cables (depending on number of channels)
- 1 Netlo 230B/C or Synaccess NP Power Distribution Unit (optional)
- 2-4 11742A Blocking Capacitors (depending on the number of selected channels)

Figure 4-5 and Figure 4-6 show how to connect the M8020A generator configuration for device tests.

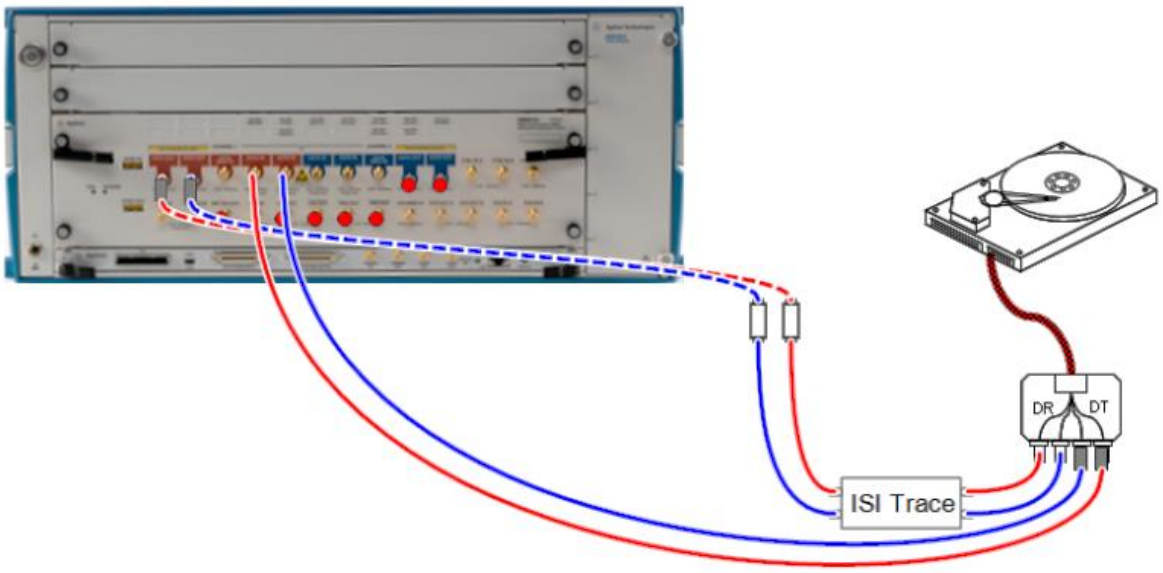

Figure 4-5: Connection Diagram for M8020A setup with 1 Channel

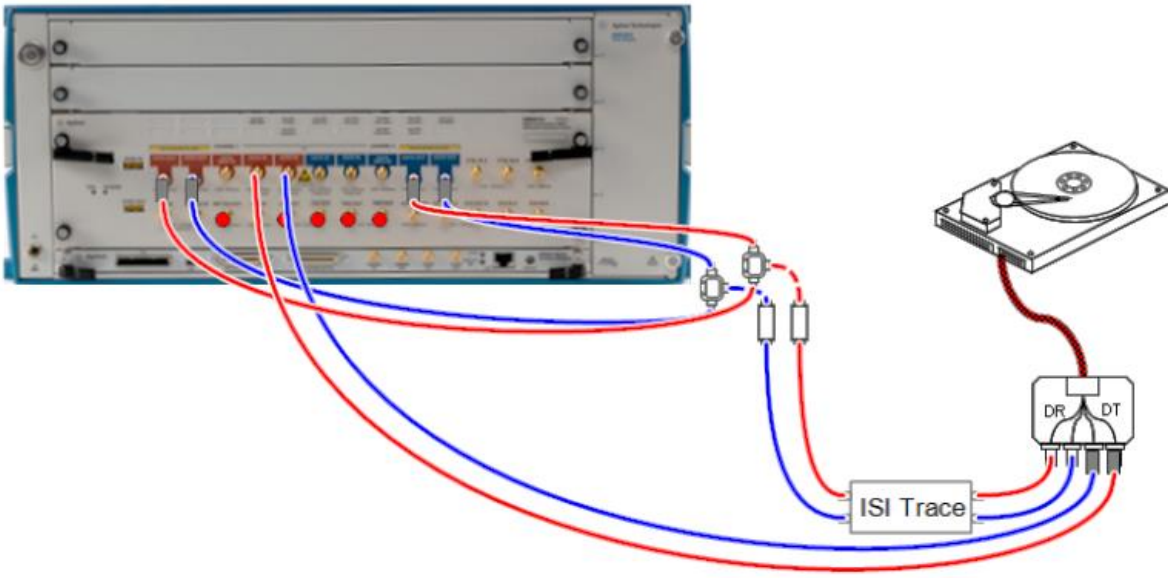

Figure 4-6: Connection Diagram for M8020A Setup with 2 Channels

4.2.1 With Trigger

When the UUT is a host, the training sequence can be started by using the trigger input as shown in Figure 4-7.

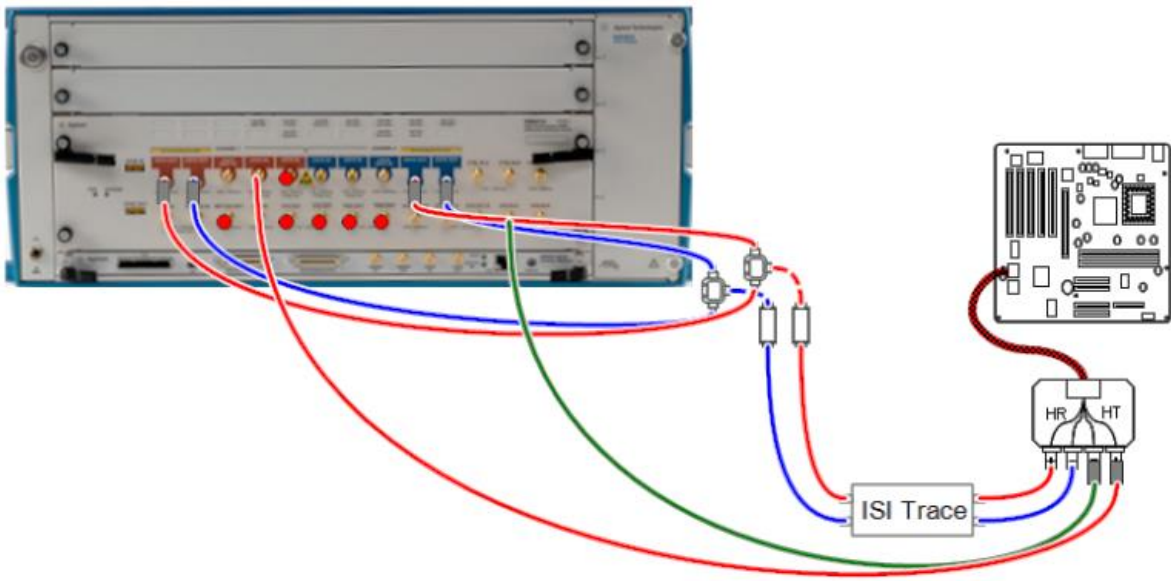

Figure 4-7: Connection Diagram for M8020A with Trigger (Host)

5 Using the Software

5.1 Connecting To The Instruments / 23
5.2 Main Window / 26

5.1 Connecting to the Instruments

Once the SATA Link Training Suite has been started, the software is in ”offline” mode. This means that user input has no effect until the software is connected to instruments. Click the “Connect...” button (see Figure 5-1) to open the connection dialog. It allows all parameters to be entered that are necessary to establish connections to the signal generator and complementary instruments.

NOTE

Suitable cable connections between the PC and the instruments are required, such as LAN or USB-to-GPIB connections. The specific connection is reflected in the name-string of the instrument. For details on naming conventions, refer to the Keysight IO Libraries.

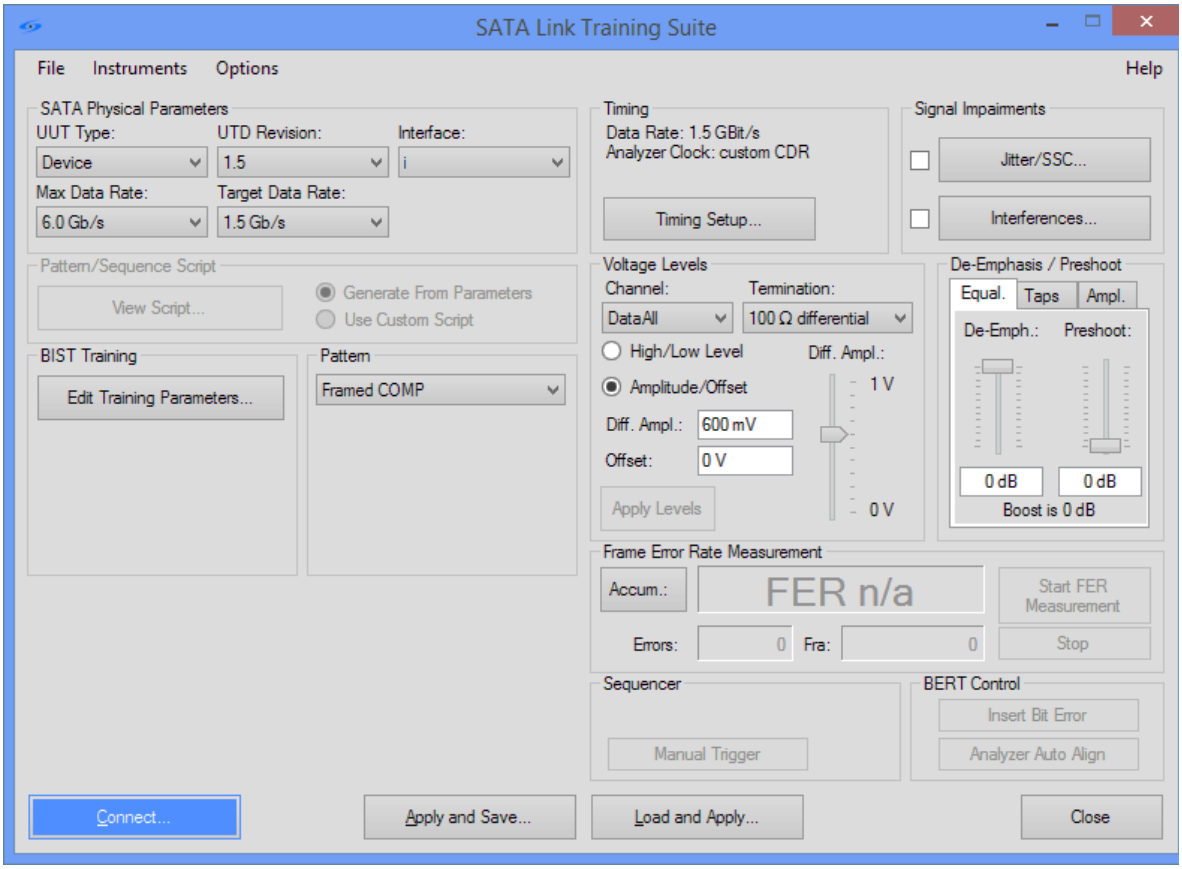

Figure 5-1: SATA Link Training Suit Main Window (Instruments Unconnected)

In the Connection Dialog window (see Figure 5-2):

1. Select the BERT configuration such as:
   - N4903B
   - M8020A
2. Select the number of data channels.
3. Enter the N4903B/M8020A connection string, which is shown by the Keysight VISA IO Connection Expert Software.
4. In the case of the N4303B generator:

Select if you want to use an N4916B De-emphasis signal converter to generate the de-emphasis signal. In order to be able to use an N4916B De-emphasis signal converter, it must be connected to the rear USB port of the J-BERT. Please refer to the N4916B Getting Started Guide when connecting an N4916B for the first time. This option is only available for one data channel.

The M8020 generates the de-emphasis internally.

5. If you have a remote-controllable power switch, check the “Power Switch” check-box and enter its address. The default address format is “IP;Username;Password”. You must also select a channel number.
6. Pressing on the “Connection Info” button displays the connection setup dialog for the selected BERT configuration.
7. After setting the desired configuration, click on the “Connect**”** button. If the Connect button is pressed, the desired connections will be checked and, if available, established.
8. Once the instruments are connected successfully, the “Initialize Instruments**”** button is enabled. Pressing the “Initialize Instruments” button applies the default configuration to the instrument(s).
9. The “Close**”** button terminates the Connection dialog window without applying any settings.

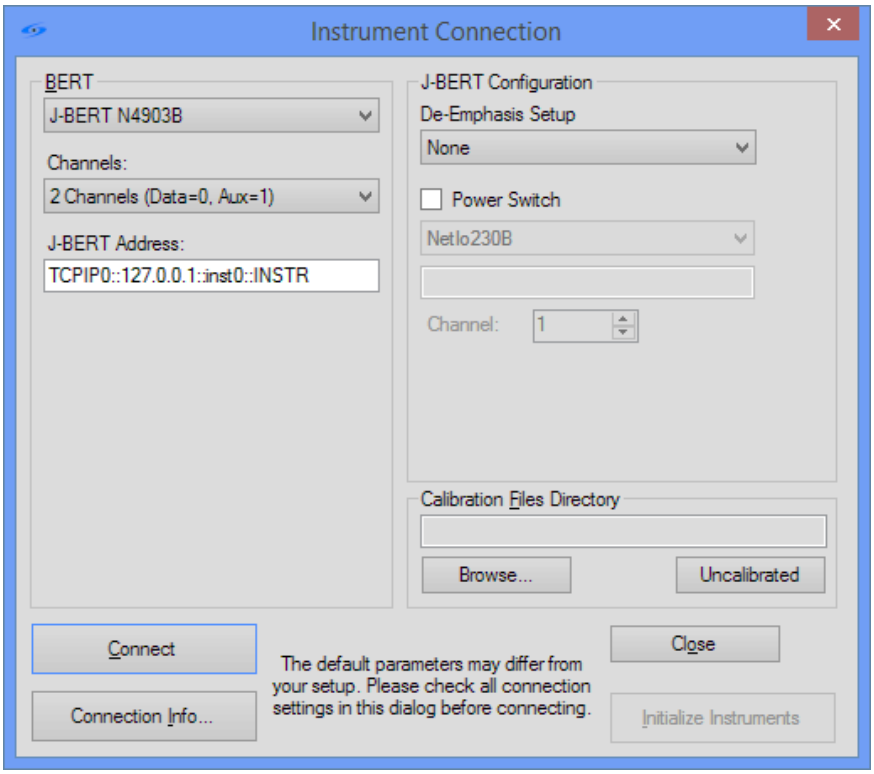

Figure 5-2: Instrument Connection Window

5.2 Main Window

After the successful connection of the instruments, the main window is displayed as given in Figure 14. This window is split into two major parts:

- The left part of the window displays SATA-specific parameters:
  - SATA Physical Parameters
  - Pattern/Sequence Script
  - BIST Training
  - Pattern
- The right part of the window displays common J-BERT parameters:
  - Timing
  - Signal Impairments
  - Voltage levels
  - De-emphasis/Preshoot
  - Frame Error Rate Measurement
  - Sequencer
  - BERT Control

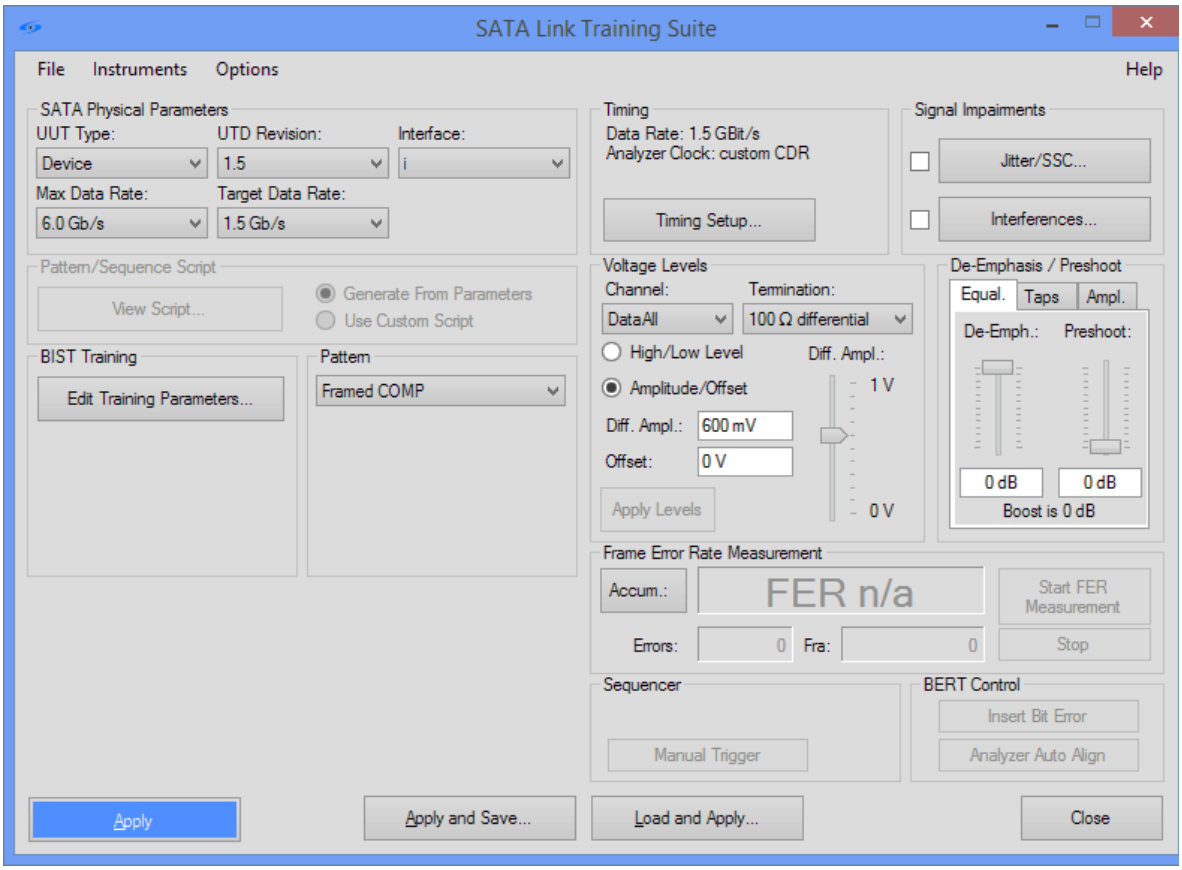

Figure 5-3: SATA Link Training Suite Main Window (Instruments connected)

After the desired parameters have been selected, the following steps (see Figure 5-3) can be done.

- Clicking on the “Apply” button sends the setup information to the instrument(s). Once this information is received by the instrument(s), the transmission of the SATA signal is started. The signal is transmitted continuously until a new setting is applied.

  Many group boxes and windows have a dedicated “Apply” button, which only applies the parameters in that group or window. There is also the menu command “Apply Pattern Only” to apply the pattern only while all other parameters remain untouched. You can find this command in the “Instruments” menu.
- Store your current settings using the “Apply and Save...” button in the main window, or via the main menu. Note that before the settings are saved, they are applied to the hardware. Only if applying succeeds can the settings be saved. This guarantees that only those settings can be saved which are in a consistent state.
- The settings can be restored at any time using the “Load and Apply...” button, or via the main menu. The restored settings are then immediately applied to the hardware.

5.2.1 Basics

The basic operation of the SATA Link Training Suite is as follows:

- Select a SATA UUT
- Select a loopback pattern
- Apply the settings to the instruments and train the unit into loopback

Now you can adjust the instrument parameters to debug your UUT, e. g. reduce the differential amplitude until frame errors are observed or deviate the data rate to test the UUT's margins.

One of the main features of the SATA Link Training Suite is the ability to modify the training sequence and the loopback pattern. You can let the SATA Link Training Suite generate those automatically, or you can fine-tune the sequence and patterns using a simple macro language.

Two terms you might encounter from time to time are "sequence" and "pattern". A pattern is a stream of bits that is sent out by the BERT. In order to be more flexible, the entire bit stream is divided into multiple patterns, which are then processed by a sequencer. The sequencer can loop patterns and step from one pattern to another. In this way, it is possible to generate very long data streams with only short patterns, which fit perfectly into the instrument's limited memory.

CAUTION

Since the SATA Link Training Suite is mainly intended for debugging and troubleshooting, the parameters are not constrained to the compliance values. Therefore, you must take care not to increase critical parameters beyond the ratings of the UUT.

5.2.2 SATA Physical Parameters

UUT Type

The unit under test Type can be selected as:

- Host
- Device

UTD Revision

It is the specification version. The available versions are:

UTD 1.2, 1.3, 1.4, 1.4.2,1.4.3 and 1.5

Interface

This can be “i” (internal), “m” (external) or “u”. “i” and “m” use different spec limits but are identical otherwise. “u” has a special calibration procedure for gen3 hosts.

Max Data Rate

Select the maximum data rate that the UUT supports.

Target Data Rate

The tested data rate.

5.2.3 BIST Training

The BIST (Build-In Self Test) training sequence is supposed to train the UUT into loopback. By default, it is generated automatically. However, you have the option to parametrize the sequence to adjust it to your UUT's needs.

When you click on “Edit Training Parameters...” (Figure 5-4), you can adjust the number of packets transmitted for every stage of the link training (see Figure 5-5).

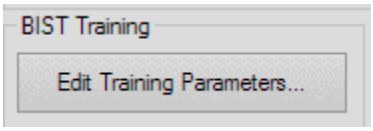

Figure 5-4: BIST Training Section

Unit Under Test

This section shows the information related to the tested UUT such as the type, the maximum supported data rate and the target data rate.

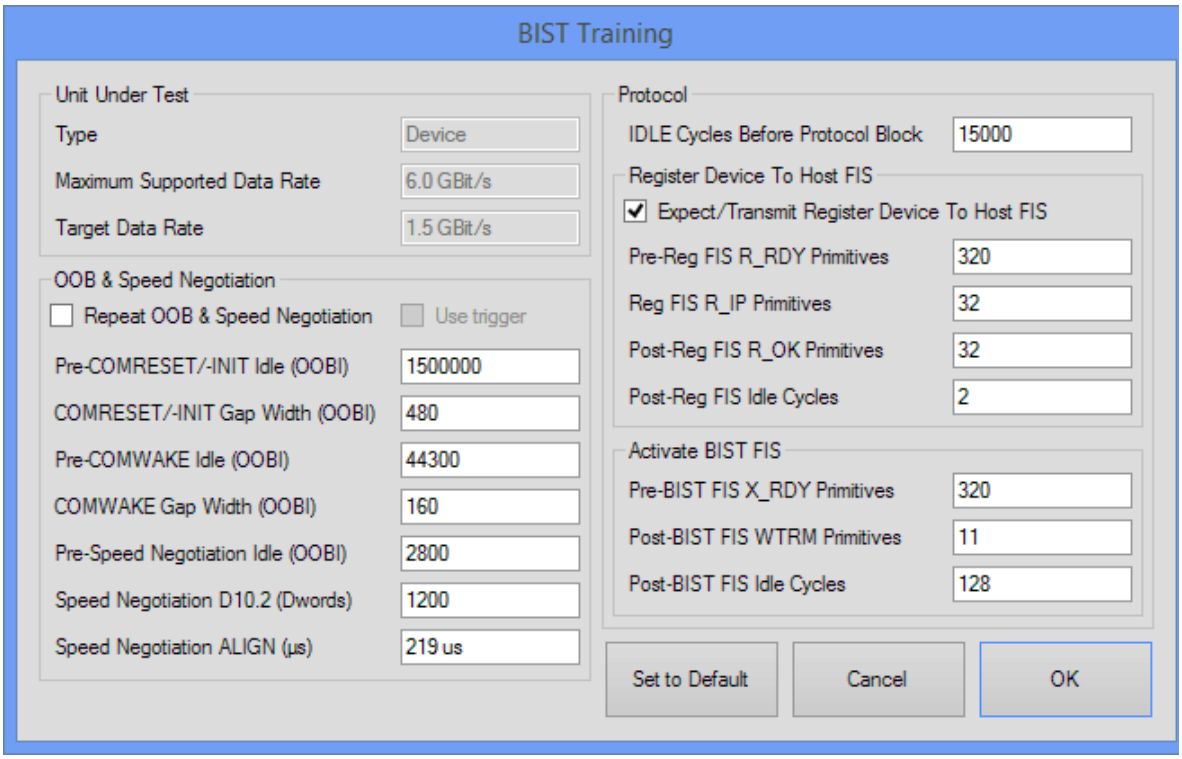

Figure 5-5: BIST Training Dialog

OOB & Speed Negotiation

This section allows the idle timings of the COMRESET/COMINIT and COMWAKE OOB (Out of Band) signals to be modified, in particular the duration of the idle signal sent before the OOB bursts and the inter-burst idle state. All OOB settings are defined in generation 1 (1.5 Gbit/s) unit intervals, also called Out Of Band Intervals (OOBIs).

The duration of the different parts of the speed negotiation can also be selected.

The “Use trigger” option is only available for Host units. If selected, the signal transmitted by the UUT is used as a trigger to start sending the Pre-OOB Idle. One of the outputs of the Host must be connected to the trigger input of the pattern generator as shown in Figure 4-4 and Figure 4-7.

Some UUTs do not correctly use the speed negotiation phase to set up the correct data rate for the BIST mode if the target data rate is not the maximum data rate they support. Those UUTs need to be “toggled down” from their maximum data rate by repeated OOB and speed negotiation. The “Repeat OOB & Speed Negotiation” option can be used to train those UUTs to the intended data rate. The required number of repetitions is automatically calculated based on the selected values of “Maximum Supported Data Rate” and “Target Data Rate”.

Protocol

This section of the software allows you to modify the composition of the protocol data that is sent to set the UUT into BIST mode. All of the protocol data is sent at the target data rate. In the protocol context an idle cycle means 254 SYNC and 2 ALIGN primitives. “Idle Cycles Before Protocol Block” controls how many of those are sent before the Register and Activate BIST frames.

The “Register Device To Host FIS” section contains settings for an optional Register Frame. Some devices always send that frame, others do not. Some hosts need to receive this frame before they accept the Activate BIST frame, others do not. The settings in this section change depending on the selected UUT type. For devices the settings control the number of R_RDY, R_IP and R_OK primitives the data generator sends while expecting the device to send its Register frame. For hosts, the settings control how many times the Register Frame itself is sent, the number of X_RDY primitives sent before the Register frame and the number of WTRM primitives sent after the Register frame. For both the host and the device cases there is an option to control the number of idle cycles sent in the end.

The Activate BIST FIS (Frame Information Structure) section contains settings for the primitives sent before and after the Activates BIST frame.

5.2.4 Pattern

The pattern that is continuously transmitted in loopback mode can be defined in the "Pattern" box, as shown in Figure 5-6.

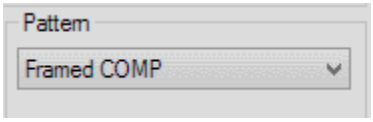

Figure 5-6: Loopback Pattern Section

The available patterns are:

- Framed COMP: This is the pattern used for compliance testing. It is a framed pattern with ALIGN pairs inserted every 256 dwords. A short Inter Gap region is introduced between EOF (End of Frame) and SOF (Stat of Frame) to ensure that ALIGN primitives are perfectly and uniformly spaced 256 dwords apart even after wrap-around by the generator. The frame contains several other test patterns in the following order: SSOP, HTDP, LTDP, LBP, LFSCP, HTDP.
- Low Frequency Test (LFTP): This pattern provides a low frequency that is allowed within the Serial ATA encoding rules. Pattern 0111 1000 1110 0001 1100b = encoded D30.3. The pattern is repetitive.
- Mid Frequency Test (MFTP): This pattern provides a middle frequency that is allowed within the Serial ATA encoding rules. Pattern 1100 1100 1100 1100 1100b = encoded D24.3. The pattern is repetitive.
- High Frequency Test (HFTP): This pattern provides the maximum frequency allowed within the Serial ATA encoding rules. Pattern 1010 1010 1010 1010 1010b = encoded D10.2. The pattern is repetitive.
- Lone Bit (LBP): This pattern comprises of the consecutive combination of certain 8b/10b encoded patterns that result in a lone bit. It creates a condition where the preceding 4 bit run-length results in minimum amplitude of the lone bit as well as its time-width in comparison to its surrounding segments. This is often the worst-case condition that the receiving data recovery circuits may encounter.
- Low Transition Density (LTDP): This pattern contains long runs of ones and zeros, intended to create inter-symbol interference by varying the excursion times at either extreme of the differential signaling levels.
- High Transition Density (HTDP): This pattern contains short runs of ones and zeros, also intended to create inter-symbol interference.
- Low Frequency Spectral Content (LFSCP): This pattern is a good test of the input high pass filter circuitry, more specifically, introduced amplitude signal distortion, due to a marginal design. These bit patterns are a better test than those bit patterns having high frequency spectral content.
- Simultaneous Switching Outputs (SSOP): This pattern is achieved by transmitting alternating one's complement bit patterns (10 bits) for recovery at the receiver. These patterns create worst case power supply, or chip substrate, noise, and are achieved by selecting bit test pattern sequences that maximize current extremes at the recovered bit pattern parallel interface. These patterns induce Ldi/dt noise into substrate supply, and are a good test of the receiver circuitry.

5.2.5 Pattern/Sequence Script

The main advantage of the Expert Mode (Option → Expert Mode) is the possibility of editing the link training sequence and pattern using a script. This allows you to define virtually any kind of pattern, whereas the methods mentioned earlier in this document only allow patterns to be generated that are in sync with the SATA link training methodology.

In order to be able to edit the script, Expert mode must be enabled, and the script must be defined as the source of the pattern. By default, the pattern that is downloaded to the generator is defined via parameters, such as the “Edit Training Parameters” box. However, in Expert Mode the group box “Pattern/Sequence Script” becomes available (Figure 5-7).

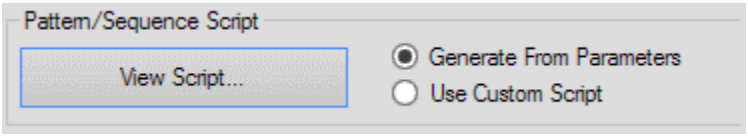

Figure 5-7: Pattern/Sequence Script Section

When the radio button “Generate From Parameters” is checked, the pattern will be automatically generated, i. e. in the same way as in non-Expert Mode. When the radio button “Use Custom Script” is checked (see Figure 5-8), a custom script will be used. The parameters for the automatically generated script are disabled then and have no influence.

To edit the script, click the “Edit Script” button. The script editor, as shown in Figure 5-9, will pop up. In the script editor, you can edit the sequence and pattern, with a unified syntax. It allows you to define the data using terms common to SATA. For example, to generate a COMRESET signal, you can use the macro “OOB_BURST(480)”. You can also use the menu to convert pattern data between different representations (binary, hexadecimal, 8b/10b).

Clicking the “Process SATA Macros” button starts a script translation, where all SATA-specific macros and symbol names are converted into their binary or 8b/10b representation.

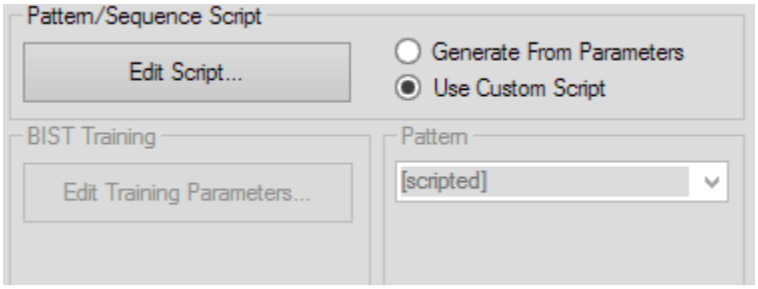

Figure 5-8: Custom Script Selected

When the “Generate From Parameters” option is used, the “Edit Script” button will change to “View Script”. In that case, the script can only be changed by modifying the parameters in the main window.

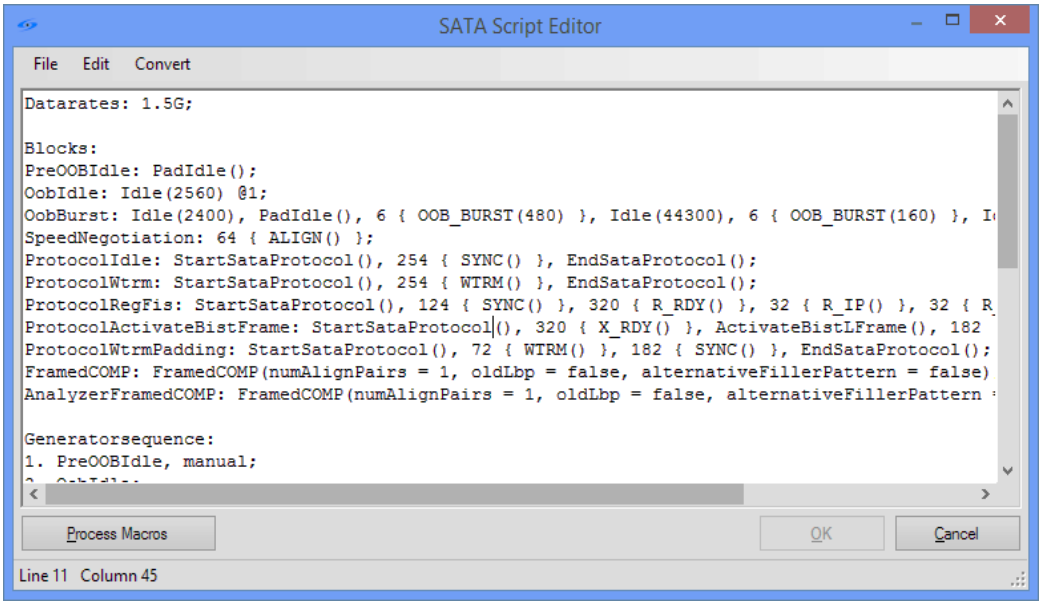

Figure 5-9: SATA Script Editor Window

Limitations

When editing the script, the resulting pattern must not violate the generator's limitations. The main limitations are the 512 bit pattern granularity in the J-BERT N4903B case and the 80 bit pattern granularity in the M8020A case.

If the pattern you want to define doesn't meet this granularity, you could, for example, repeat the pattern until the granularity is met (using the {} operator), or place a Pad0() macro somewhere to stuff the pattern with zeros. For more details about the language syntax, please refer to the “SATA Link Training Suite Language Guide”.

5.2.6 Exporting the Script

Once you have found a link training sequence suitable for your needs, you may want to export this sequence, either for later use or to the automated test solution software.

To export the current script, click “File”, then “Export Script”. This saves the currently used script for the training sequence to a file, regardless of whether you defined it via parameters or by editing the SATA or generic script.

5.2.7 Timing

Click “Timing Setup” button (see Figure 5-10) to open the timing setup window as shown in Figure 5-11.

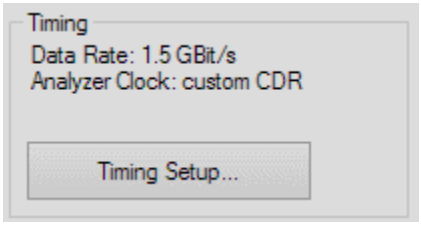

Figure 5-10: Timing Section

Here you can define the data rate and add some deviation to it. The reference clock can also be modified, but keep in mind that the valid range and granularity are restricted by the generator hardware. By default, the generator uses an internal clock source.

You can configure the analyzer's clock to external clock or clock data recovery (CDR). When CDR is selected parameters such as Loop Bandwidth, Peaking, and Expected Transition Density can be modified.

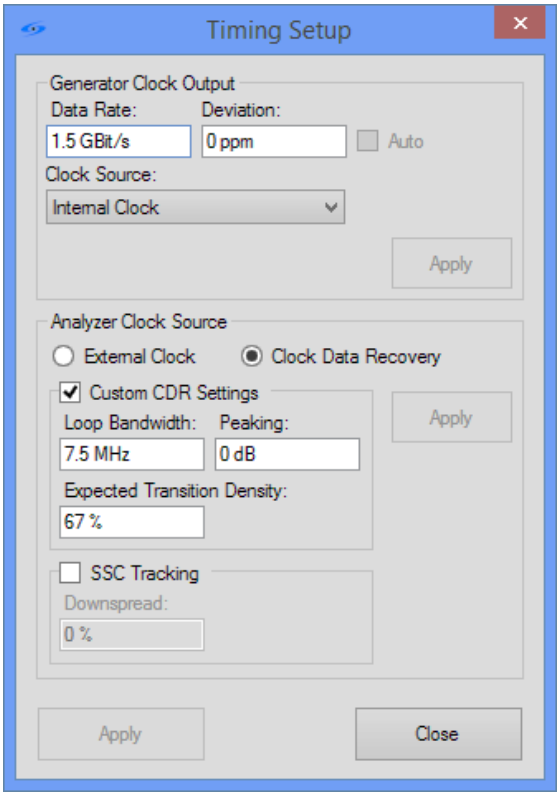

Figure 5-11: Timing Setup Window

5.2.8 Signal Impairment

Jitter Setup

Click on the "Jitter/SSC" button (see Figure 5-12) to open the jitter setup window as shown in Figure 5-13.

The dialog allows different types of jitter to be defined when the hardware jitter sources are available:

- Spread Spectrum Clocking (SSC)
- Sinusoidal Clock Jitter
- Periodic Jitter
- Compliance Spectral RJ

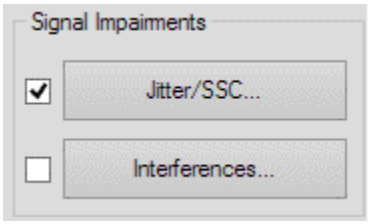

Figure 5-12: Signal Impairment Section

The parameter values can be entered either by selecting the parameter field with a left mouse-button click and using the slider or manually. When any slider is moved, the corresponding parameter will be written to the hardware immediately. Otherwise, you'll have to click the “Apply” button. When you change any parameter, for example enter a new value in a text-box, the corresponding “Apply” button is highlighted. This means that you have to click on Apply in order to activate your changes.

Note that some jitter/SSC parameters will reset the sequencer when modified. This means that the current sequencer state is left and the link training is restarted.

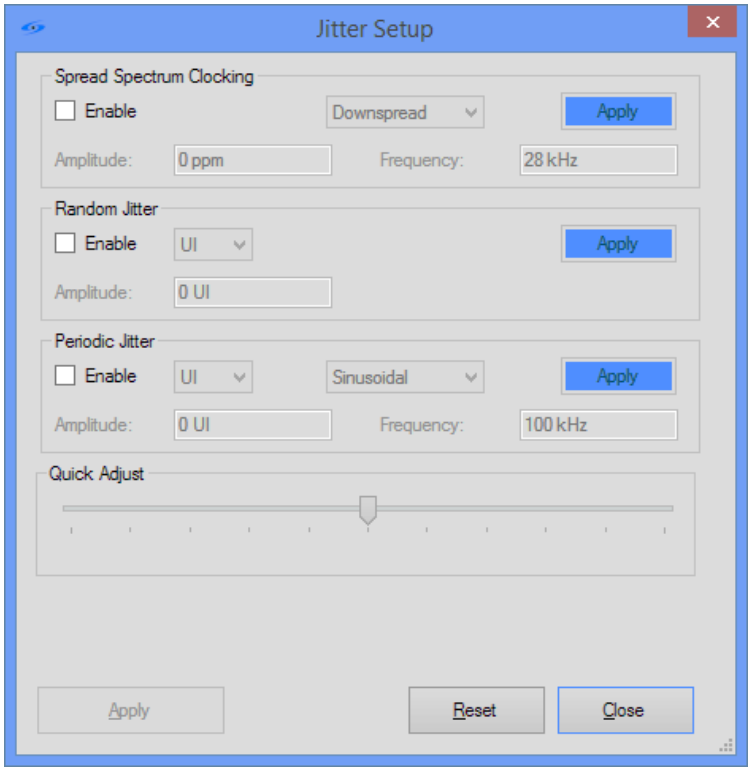

Figure 5-13: Jitter Setup Window

Interferences

Click the "Interferences..." button (see Figure 5-12) to open the interferences window as shown in Figure 5-14. You can modify the common-mode and differential-mode sinusoidal interferences.

If you are using the J-BERT N4903B as the pattern generator, common-mode interference is generated with the J-BERT N4903B J20 module. Use of the J20 cannot be combined with differential-mode interference.

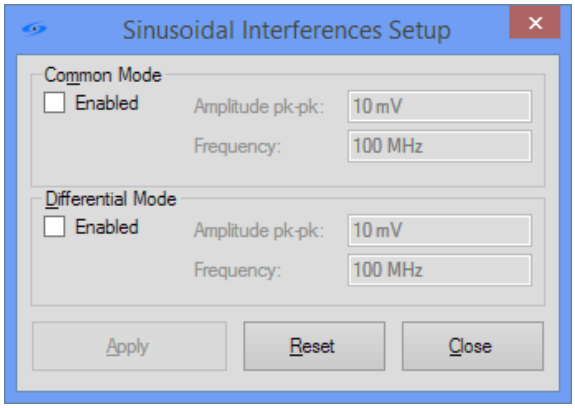

Figure 5-14: Sinusoidal Interference Setup Window

5.2.9 Voltage Levels

The data channel levels can be modified in the Voltage Levels Panel (Figure 5-15). The parameter values can be entered numerically or by using the slider. If the parameter values are entered numerically, the “Apply Levels” button needs to be pressed to apply the values. If the slider is moved to change the values, the levels are applied instantaneously. The levels can be set for each data channel individually. The default values for the data channels are 0 V offset and 600 mV differential amplitude.

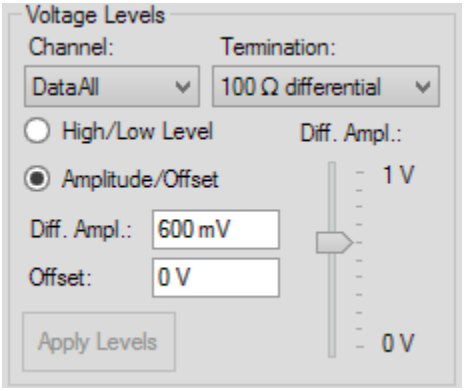

Figure 5-15: Voltage Levels Selection Section

5.2.10 De-Emphasis/Preshoot

If a De-Emphasis generator source is available, you can control the de-emphasis and preshoot levels as shown in Figure 5-16.

The tabs let you select from three different views:

- de-emphasis and pre-shoot in dB
- FIR tap coefficients
- emphasized and de-emphasized voltage levels

Note that when any slider is moved, the corresponding parameter will be written to the hardware immediately. Otherwise, you will have to click the “Apply” or “Apply Levels” button.

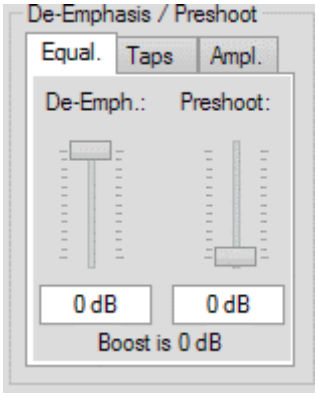

Figure 5-16: De-Emphasis Section

5.2.11 Frame Error Rate Measurement

You can click the "Start FER Measurement" (Figure 5-17) in the right part of the window to automatically poll the frame and error counters of the error detector used. By default, the displayed FER (Frame Error Rate) is calculated from the total number of frames and total number of errors. You can click the button on the left side of the FER display to toggle to the current FER, which is the calculated FER of the last error counter reading. Note that neither of these number is necessarily always equal to the FER displayed in the J-BERT/M8020, since the measurement intervals might be different.

You can click "Reset FER Measurement" to reset the symbol- and error-counter.

The FER can be used to determine whether link training was successful or not. A very high FER and increasing error count could indicate that no link training was performed, because the error counter is always programmed to compare the only loopback pattern.

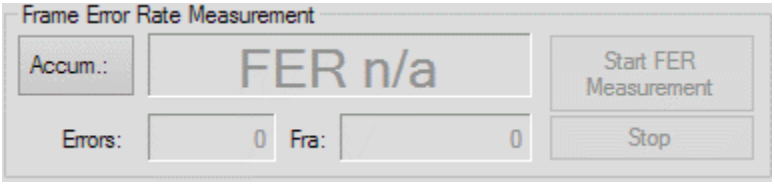

Figure 5-17: FER Measurement Section

5.2.12 BERT Control

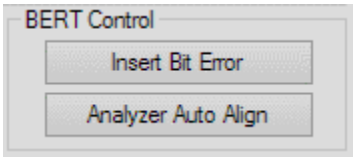

Figure 5-18: BERT Control Section

Insert Bit Error

The “Insert Bit Error” option of the BERT Control section (see Figure 5-18) causes the generator to insert a single bit error into the data stream. This can be useful to verify that the UUT is in loopback; when the UUT is not in loopback, inserting bit errors does not affect the bit error and BER counters.

Analyzer Auto Align

The “Analyzer Auto Align” button is used to conduct a bit alignment of the BERT analyzer. For a comparison of the incoming pattern with the pattern in the analyzer, the clock of the TX (Transmitter) side of the UUT and the analyzer clock must be in phase. This is ensured by a common reference clock. When the received bits are not synchronized with the pattern of the analyzer, the computed BER will be very high. In this case, clicking on the “Analyzer Auto Align” button restarts the synchronization algorithm in the analyzer.

5.2.13 Sequencer

The group box in Figure 5-19 shows the sequencer control.

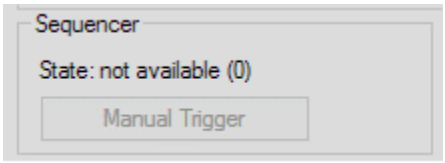

Figure 5-19: Sequencer Section

When the “Poll Sequence State” option in the “Options” menu is enabled, the current state of the sequencer is shown.

When the sequence contains a loop with a manual break condition, that loop can be ended with the “Manual Trigger” button.

6 Troubleshooting and Support

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6.1 Startup Fails

The anti-virus software Sophos Endpoint Security mistakenly classify detect the SATA Link Training Suite as a virus and prevent it from executing. Starting the Link Training Suite then leads to an error message such us "*Windows cannot access the specified device, path, or file*". In this case, please check whether the anti-virus software blocked the executable file of the SATA Link Training Suite and add it to the exceptions. Note that you will probably have to repeat this procedure for some of the DLLs.

6.2 Slow Response

If you encounter a slow response of the SATA Link Training Suite user interface, this might be a result of a poor remote connection. Probably the delay over Ethernet is too high.

In most cases, it helps to disable the FER polling and the sequencer status polling. The FER polling can be disabled by simply clicking the "Stop" button in the "Frame Error Rate Measurement" group. The sequencer state polling can be disabled by un-checking the "Poll Sequence Status" item in the "Options" menu.

6.3 Link Training Fails

If link training fails, you might want to check the following points:

Did you already click "Apply" after connecting and adjusting all your parameters? Note that just connecting doesn't automatically download the pattern and settings!

Is the injected jitter too high? Try reducing or disabling the injected jitter in the "Jitter/SSC" dialog.

Are the timing, the voltage levels, and the de-emphasis correct?

Is the selected link training sequence suitable for your UUT? Probably using a tweaked sequence helps your UUT to get into loopback.

This information is subject to change without notice.
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